CLAIMS

What is claimed is:

1. A memory comprising:

an x-direction driver set;

a y-direction driver set;

a plurality of x-direction conductive array lines formed above both driver sets and being electrically connected to the x-direction driver set, the electrical connection occurring substantially in the middle of the x-direction conductive array lines;

an array cut in the plurality of x-direction conductive array lines, the array cut being where two contiguous x-direction conductive array lines are spaced further apart than other contiguous x-direction conductive array lines;

a plurality of memory plugs formed above the plurality of x-direction conductive array lines and in electrical contact with the plurality of x-direction conductive array lines;

a plurality of y-direction conductive array lines formed above the plurality of memory plugs and being electrically connected to the y-direction driver set, the electrical connection occurring over the array cut and being substantially in the middle of the y-direction conductive array lines.

2. The memory of claim 1, wherein:

the x-direction driver set has an edge that is substantially aligned with the middle of the x-direction conductive array lines, whereby the edge divides the x-direction conductive array lines into a first portion and a second portion.

3. The memory of claim 2, wherein:

the x-direction driver set has two portions, both portions having an edge that is substantially aligned with the middle of the x-direction conductive array lines, the first portion being arranged to be substantially underneath the first portion of the x-direction conductive array lines, and the second portion being arranged to be substantially underneath the second portion of x-direction conductive array lines.

4. The memory of claim 3, wherein:

the two portions of the x-direction driver set are approximately equal in size.

5. The memory of claim 2, wherein:

the y-direction driver set has an edge that is substantially aligned with the middle of the y-direction conductive array lines, whereby the edge divides the y-direction conductive array lines into a first portion and a second portion..

6. The memory of claim 5, wherein:

the y-direction driver set has two portions, both portions having an edge that is substantially aligned with the middle of the y-direction conductive array lines, the first portion being arranged to be substantially underneath the first portion of the y-direction conductive array lines, and the second portion being arranged to be substantially underneath the second portion of y-direction conductive array lines.

7. The memory of claim 6, wherein:

the two portions of the y-direction driver set are approximately equal in size.

8. The memory of claim 1, wherein:

the y-direction driver set has an edge that is substantially aligned with the middle of the y-direction conductive array lines.

9. A device comprising:

a semiconductor substrate; and

a stacked cross point array formed over the semiconductor substrate, the stacked cross point array having at least two layers of memory cells, each successive layer of memory cells being formed over the previous layer of memory cells;

wherein the stacked cross point array has at least two separate access times, the fastest of which is associated with the layer of memory cells closest to the semiconductor substrate.

10. The device of claim 9, wherein:

the stacked cross point array has only two separate access times.

11. A device comprising:

a stacked cross point having

a first x-direction conductive array line layer;

a first memory plug layer having a first access time, and positioned on top of the first x-direction conductive array line layer;

a first y-direction conductive array line layer on top of the first memory plug layer;

a second memory plug layer having a second access time, and positioned on top of the first y-direction conductive array line layer; and

a second x-direction conductive array line layer on top of the second memory plug layer;

wherein the first access time is faster than the second access time.

12. The device of claim 11, wherein:

the memory plug layers exhibit a non-linear resistive characteristic.

13. The device of claim 12, wherein:

the resistive memory elements are formed from conductive metal oxides.

14. The device of claim 11, wherein:

the device is part of a re-writable memory.